In The Claims:

Claim 1. (currently amended) A pixel structure, comprising:

a gate line, located on a substrate;

a common line, located on said substrate for a bottom electrode of a pixel storage capacitor;

a gate insulating layer, located on said substrate, said gate insulating layer covering said gate line and said common line;

a data line, located on said gate insulating layer;

a switching device, located on said substrate, said switching device electrically connecting said gate line and said data line;

a conducting layer, located on said gate insulating layer, said conducting layer including a coupling portion and a connecting portion, said coupling portion being above said common line for a top electrode of said pixel storage capacitor, said connecting portion comprising a first portion, a second portion and the third portion, wherein said first portion is coupled to said coupling portion, said second portion is connected to said switching device and said third portion located between said first portion and said second portion possesses a plurality of channels ~~connecting said coupling portion and said switching device~~;

a passivation layer, covering said data line, said switching device, and said conducting layer;

a contact window, disposed in said passivation layer and above said third portion of said connecting portion; and

a pixel electrode, located on said passivation layer, said pixel electrode electrically connecting said switching device and said coupling portion of said conducting layer

through said contact window.

Claims 2-3 (canceled)

Claim 4. (original) The pixel structure of claim 1, further comprising a blocking layer below said connecting portion.

Claim 5. (original) The pixel structure of claim 1, further comprising a planarization layer between said passivation and said pixel electrode.

Claim 6. (original) The pixel structure of claim 1, wherein said switching device is a thin film transistor, said thin film transistor comprising:

a gate electrode electrically connected to said gate line;

a channel layer on the gate insulating layer above said gate electrode;

a source electrode and a drain electrode on said channel layer, said source electrode being electrically connected to said data line, said drain electrode being electrically connected to said connecting portion of said conducting layer.

Claim 7. (original) The pixel structure of claim 1, wherein said gate line is parallel to said common line.

Claim 8. (currently amended) A method of fabricating a pixel structure, comprising

sequentially forming a gate electrode a gate line and a common line on a substrate,

wherein the gate line is electrically connected to said gate electrode;

forming a gate insulating layer on said substrate to cover said gate electrode, said gate line and said common line;

forming a channel layer above said gate insulating layer and said gate electrode;

forming a data line and a conducting layer on said gate insulating layer and forming a source electrode and a drain electrode on said channel layer, said data line being electrically connected to said source electrode, said conducting layer including a coupling portion and a connecting portion, said coupling portion being formed above said common line, said connecting portion connecting said coupling portion and said drain electrode, wherein said connecting portion comprises a multi-channel portion and said multi-channel portion possesses a plurality of channels;

forming a passivation layer above said substrate covering said data line, said conducting layer and said thin film transistor;

forming a contact window in said passivation layer exposing said multi-channel portion of said connecting portion; and

forming a pixel electrode on said passivation layer, said pixel electrode being electrically connected to said conducting layer through said contact window.

Claim 9 (canceled)

Claim 10. (currently amended) The method of claim ~~9~~ 8, wherein said contact window exposes ~~one of plurality of channels~~ at least a channel of said connecting portion.

Claim 11. (original) The method of claim 8, further comprising forming a

blocking layer below said contact window and said connecting portion.

Claim 12. (original) The method of claim 11, wherein said blocking layer is formed in a common area during forming said gate electrode, said gate line, and said common line..

Claim 13. (original) The method of claim 8, before the step of forming said pixel electrode, further comprising forming a planarization layer on said passivation..

Claim 14. (original) The method of claim 8, wherein common line is parallel to said gate line.

Claim 15. (new) A pixel structure, comprising:

a gate line located on a substrate;

a common line located on the substrate for a bottom electrode of a pixel storage capacitor;

a blocking layer located on the substrate between the gate line and the common line;

a gate insulating layer located over the substrate;

a data line located on the gate insulating layer;

a switching device located on the substrate, wherein the switching device is electrically connected to the gate line and the data line;

a conducting layer located on the gate insulating layer, wherein the conducting layer includes a coupling portion and a connecting portion, the coupling portion is located

above the common line for a top electrode of the pixel storage capacitor and the connecting portion is connected to the coupling portion and the switching device and is located above the blocking layer;

a passivation layer covering the data line, the switching device, and the conducting layer;

a contact window disposed in the passivation layer and the gate insulating layer above the connecting portion, wherein the contact window exposes a portion of the blocking layer and a portion of the connecting portion over the exposed blocking layer; and

a pixel electrode located on the passivation layer, wherein the pixel electrode is electrically connected the switching device to the coupling portion of the conducting layer through the portion of the connecting portion exposed by the contact window and the pixel electrode is in contact with the portion of the blocking layer exposed by the contact window.

Claim 16. (new) The pixel structure of claim 15, wherein the connecting portion of the conducting layer is a multi-channel structure, the connecting portion comprising:

a first portion coupled to the coupling portion;

a second portion connected to the switching device; and

a third portion between the first portion and the second portion, the third portion including a plurality of channels.

Claim 17. (new) The pixel structure of claim 16, wherein the contact window is disposed in the passivation layer and above one of the plurality of channels of the third

portion.

Claim 18. (new) The pixel structure of claim 15, further comprising a planarization layer between the passivation and the pixel electrode.

Claim 19. (new) The pixel structure of claim 15, wherein the switching device is a thin film transistor, the thin film transistor comprising:

a gate electrode electrically connected to the gate line;

a channel layer on the gate insulating layer above the gate electrode;

a source electrode and a drain electrode on the channel layer, the source electrode being electrically connected to the data line, the drain electrode being electrically connected to the connecting portion of the conducting layer.

Claim 20. (new) The pixel structure of claim 15, wherein the gate line is parallel to the common line.